with $I_m(\cdot)$ the modified Bessel functions of order m. If the mixed signal is assumed to be terminated by Z_L

$$V_{Gmix} = -Z_L I_{Gmix}. \tag{A.4}$$

From (A.1) and (A.4), a relation between $V_{G\,sig}$ and $V_{G\,mix}$ is obtained

$$V_{Gmix} = k_1 V_{Gsig} \tag{A.5}$$

where

$$k_1 = Z_{21}Z_L/(Z_{11}Z_L - Z_{12}Z_{21} + Z_{22}Z_{11}). \tag{A.6}$$

On the other hand, the relation between the gate voltage and the junction voltage is

$$\begin{bmatrix} V_{Gsig} \\ V_{Gmix} \end{bmatrix} = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \cdot \begin{bmatrix} I_{Gsig} \\ I_{Gmix} \end{bmatrix} + \begin{bmatrix} V_{Jsig} \\ V_{Jmix} \end{bmatrix}$$
$$= \left[\begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \cdot \left[\begin{bmatrix} j\omega C & 0 \\ 0 & j\omega C \end{bmatrix} + \begin{bmatrix} g_0 & g_1 \\ g_1 & g_0 \end{bmatrix} \right] + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \right] \cdot \begin{bmatrix} V_{Jsig} \\ V_{Jmix} \end{bmatrix}. \tag{A.7}$$

Therefore

$$\begin{bmatrix} V_{Jsig} \\ V_{Jmix} \end{bmatrix} = (K) \cdot \begin{bmatrix} V_{Gsig} \\ V_{Gmix} \end{bmatrix} \tag{A.8}$$

where

$$(K) = \begin{bmatrix} K_{11} & K_{12} \\ K_{21} & K_{22} \end{bmatrix}$$
$$= \left[\begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \left[\begin{bmatrix} j\omega C & 0 \\ 0 & j\omega C \end{bmatrix} + \begin{bmatrix} g_0 & g_1 \\ g_1 & g_0 \end{bmatrix} \right] + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \right]^{-1}. \tag{A.9}$$

From (A.5) and (A.8), the mixed signal and the input signal voltage at the junction are obtained as

$$\begin{bmatrix} V_{Jsig} \\ V_{Jmix} \end{bmatrix} = \begin{bmatrix} K_{11} & K_{12} \cdot k_1 \\ K_{21} & K_{22} \cdot k_1 \end{bmatrix} \begin{bmatrix} V_{Gsig} \\ V_{Gsig} \end{bmatrix}. \tag{A.10}$$

It is clear that the MESFET output signal is determined by the junction voltage. Therefore, the output signal normalized to V_{Gsig} is

$$V_{sig} = |V_{Jsig}|/|V_{Gsig}| = |K_{11} + K_{12}k_1|$$
$$V_{mix} = |V_{Jmix}|/|V_{Gsig}| = |K_{21} + K_{22}k_1|. \tag{A.11}$$

The ratio m, which is defined by (9), is

$$m = V_{sig}/V_{mix} = |K_{11} + K_{12}k_1|/|K_{21} + K_{22}k_1|. \tag{A.12}$$

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Short Papers

Submicrometer Self-Aligned GaAs MESFET

P. BAUDET, M. BINET, AND D. BOCCON-GIBOD

***Abstract*—This short paper presents a self-aligned technique which permits the production of submicrometer gate lengths and spacings between contacts. The exclusive use of standard photolithographic techniques makes this method interesting. Microwave measurements are reported for such a device with a 0.7-μm gate length in a 2.2-μm drain-source spacing. The yield of the process is usually better than 80 percent.**

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The authors are with the Laboratories of Electronics and Applied Physics, 3 Avenue Descartes, Limeil Brévannes, France.

INTRODUCTION

Since 1968 the improvement of the GaAs MESFET has required the use of smaller and more refined geometries. Thus alignment rapidly became one of the major problems in the process. To solve this difficulty, several laboratories have proposed various self-aligned methods [1]–[3]. But except for Middelhoek [4], nobody, to our knowledge, has published a self-aligned method which allows the realization of submicrometer gate and spacing contact lengths. The purpose of this short paper is to describe a new and simple method of self-alignment which does not necessitate the use of electron-beam technology.

Whereas the other methods generally use self-alignment from source and drain contacts by using the undercutting or over-

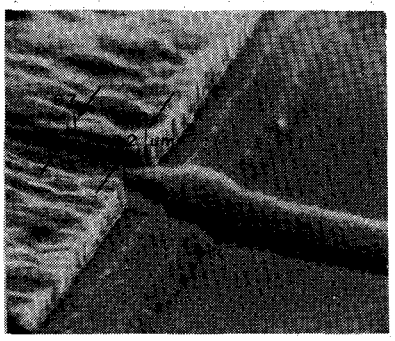

Fig. 1. Scanning-electron micrograph of a MESFET detail at the end of the channel.

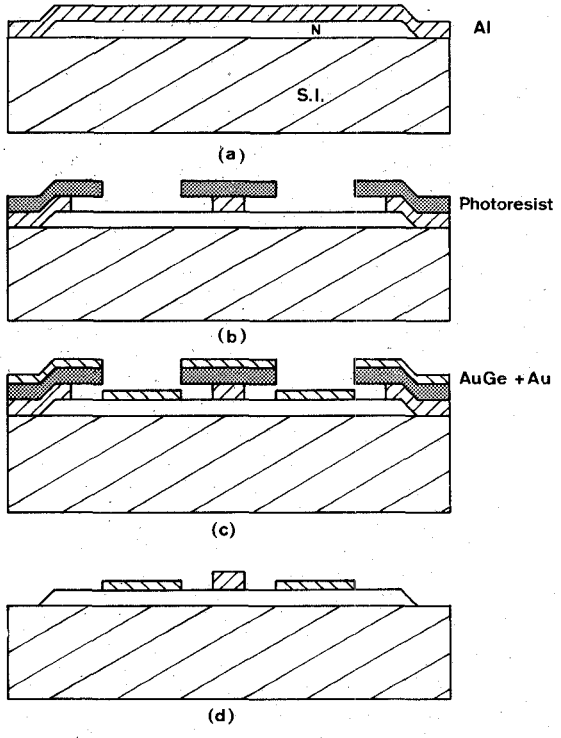

Fig. 2. Process steps of the submicrometer self-aligned GaAs MESFET.

flowing of ohmic contacts, in our method the engraving of the gate itself is used to self-align the source and drain contacts, eliminating in that way the main difficulties of the self-alignment. Such difficulties include:

1) inhomogeneities of the thickness of the layer which give a poor processing yield after making the layer thin under the gate;
2) control of the current flowing through the channel during the etching;
3) quality of the Schottky diode.

Device Fabrication

The process is carried out in the following way.

1) The starting material is a chromium-doped semi-insulating substrate on which is grown ($AsCl_3/Ga/H_2$ system) a layer of n-type material of thickness 0.15 μm–0.2 μm and doping between 8 and 10 $\times$ 10^{16} cm^{-3}. The surface of the material is a [0,0,1] plane, 3° off towards the [1,1,0] direction. The active zones of transistors are insulated by 0.4-μm-deep chemical etching. During this step the wafer is oriented so that the gate passes over a sloping mesa edge (Fig. 1).

2) In order to obtain a good diode, it is necessary to minimize the thickness of the interfacial layer between the aluminum and the n-layer, thus producing an ideality factor which approaches unity [5]. This is effected by using a classical desoxydizing treatment of the GaAs surface, after which aluminum is deposited under high vacuum.

3) The wafer is then covered with photoresist which is subsequently removed from the source and drain areas, thus defining the channel length. The source and drain areas are opened by etching the aluminum. This etching is continued until the undercutting of the aluminum is 1/3 of the channel length [Fig. 2(b)].

4) After an adequate cleaning of the GaAs surface (see paragraph 2)), an AuGe layer and an Au layer are evaporated on the wafer. The overhanging of the photoresist ensures the automatic alignment of the contacts. The photoresist is removed by a lifting process [Fig. 2(c)].

5) A final engraving of the aluminum defines a gate pad at one end of the channel. Annealing at 450°C under H_2 flow makes the drain and source contacts ohmic [Fig. 2(d)].

Results—Performances

By using this method we have made a 0.3-μm gate length in a 1.5-μm drain-source spacing (Fig. 3). These last tests were not carried out on a MESFET material and showed only that it was possible to fabricate gates as short as 0.3 μm.

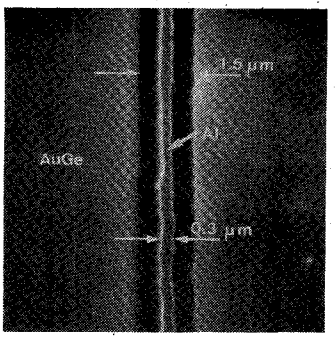

Fig. 3. Scanning-electron micrograph of a 0.3-μm aluminum gate in a 1.5-μm AuGe source to drain spacing.

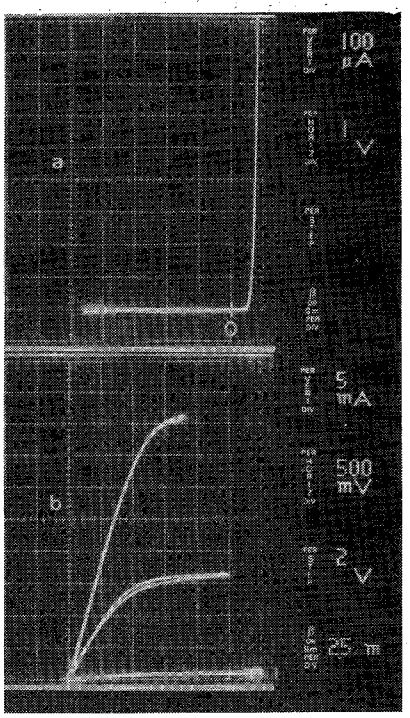

Fig. 4. (a) Typical I–V characteristic of the Schottky-barrier gate. (b) Typical I–V characteristic of a submicrometer self-aligned GaAs MESFET.

However, we report here the microwave performance obtained with this process for transistors with a 0.7-μm gate length in a 2.2-μm drain-source spacing. The channel width is 200 μm. Several wafers have been processed with success which give a yield better than 80 percent.

The characteristics $I_{GS} = f(V_{GS})$ and $I_{DS} = f(V_{DS},V_{GS})$ are shown in Fig. 4. The contact resistances are typically between 5 and 10 Ω for a 200-μm gate width. The S-parameter characterization is made with an HP network analyzer through X band. For these measurements the transistor chip is inserted in the middle of a 4-mm-long microstrip test fixture. Typical common source S-parameters are plotted in Fig. 5 for two different biases corresponding to the maximum gain [Fig. 5(a)] and minimum noise figure [Fig. 5(b)]. A fairly high value of forward transducer gain $|S_{21}|^2 = 2.8$ dB at 12 GHz is obtained for the bias conditions [Fig. 5(a)]. This is accompanied by a high reverse transducer loss which is in excess of 28 dB at this frequency.

The stability factor is larger than unity throughout X band.

To facilitate the use of the transistor we also mounted some chips on a special mount (Fig. 6). For direct measurements of gain and noise this mount is inserted into a slotted semirigid coaxial cable. In this manner we obtained the results shown in Fig. 6 by matching the input and output with double slug tuners. We measured a matched gain of 8.5 dB at 12 GHz. With the transistor matched for the minimum noise figure, the gain is 6 dB with associated noise figure equalling 4.7 dB at 12 GHz.

Fig. 7 shows the output power performance at $f = 10$ GHz of the same transistor. The matched small-signal gain was 10 dB and a power output of 3.3 mW was obtained at 1-dB gain compression. By tuning the output for maximum power, the output power was considerably increased up to 28 mW at 1-dB gain compression with an associated small-signal gain of 6.6 dB. The power output at 0-dB gain was a little larger than 40 mW.

Conclusions

We have shown that it is possible to realize a self-aligned MESFET with a submicrometer gate using standard photolithographic techniques. The results for the 0.7-μm gate length are similar to previously published results and will certainly be improved with a better quality of material and better contact resistances. In addition, the realization of gates as small as 0.3 μm will yield sufficient gain for operation in Ku band in the near future.

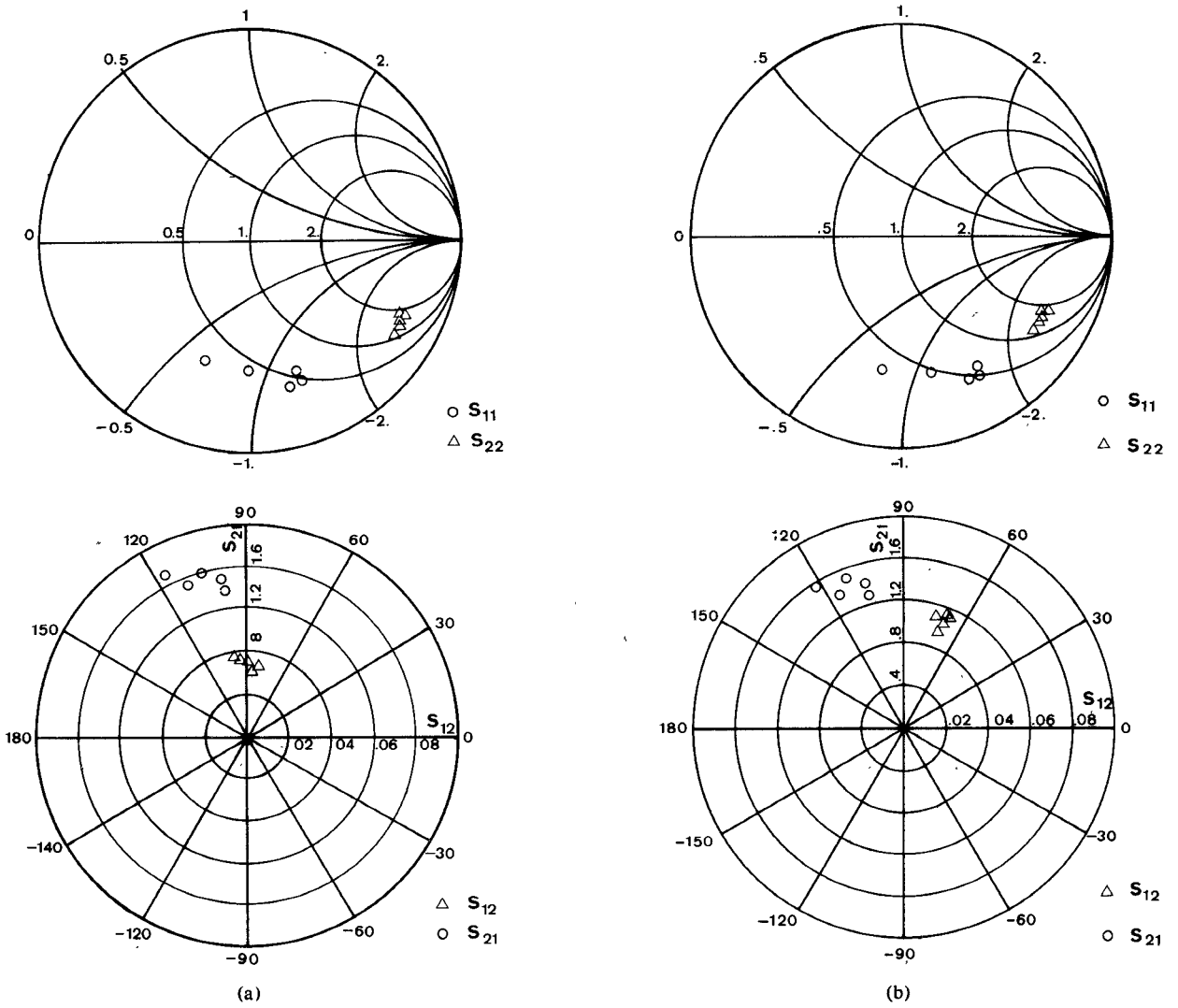

Fig. 5. (a) Measured S-parameters at 8, 9, 10, 11, and 12 GHz for a bias yielding MAG (V_{DS} = 3.75 V, I_{DS} = 44 mA). (b) Measured S-parameters at 8, 9, 10, 11, and 12 GHz for a bias yielding minimum noise figure (V_{DS} = 2.7 V, I_{DS} = 18 mA).

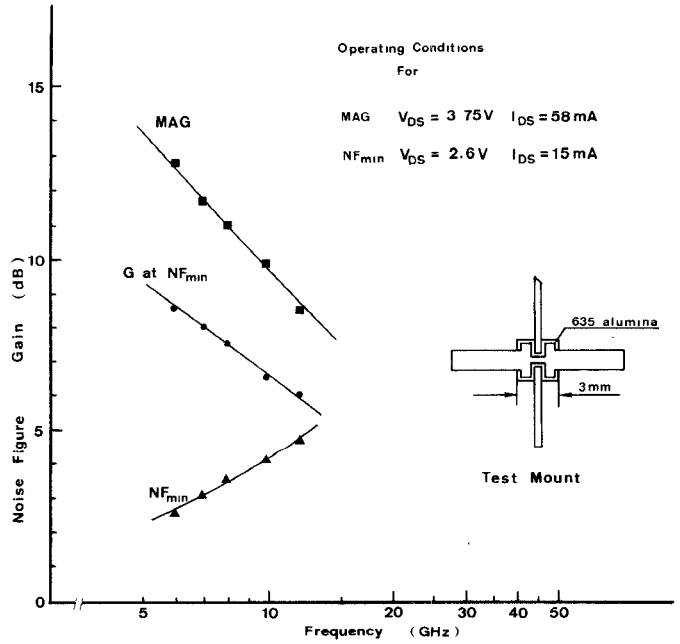

Fig. 6. Maximum available gain, noise figure, and associated gain versus frequency as measured in the test mount.

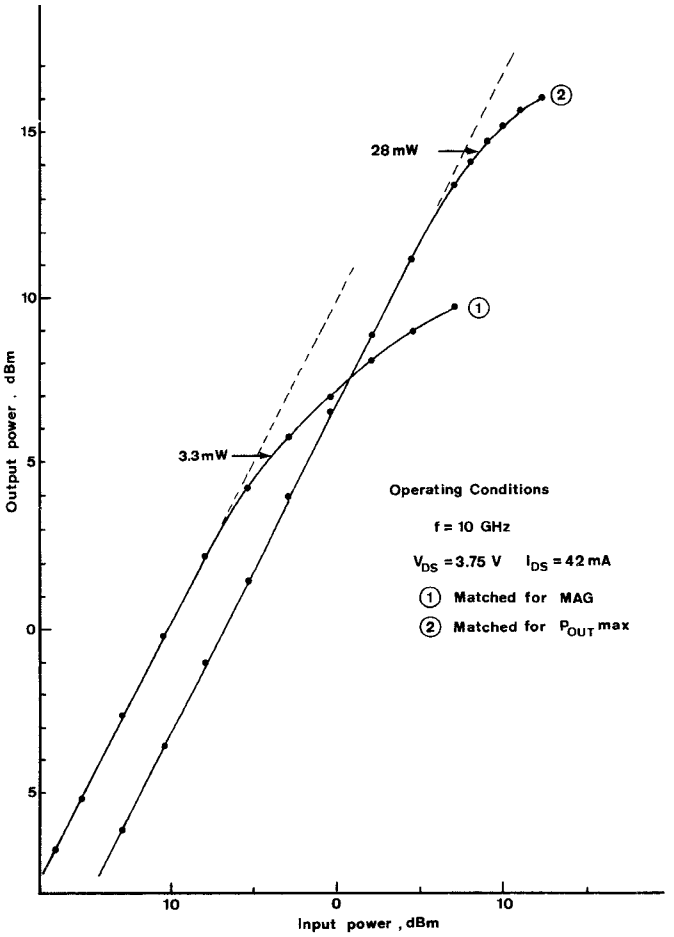

Fig. 7. Power output performance of a MESFET.

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Performance of GaAs MESFET's at Low Temperatures

CHARLES A. LIECHTI, SENIOR MEMBER, IEEE, AND
RODERIC B. LARRICK

***Abstract*—The noise- and *s*-parameters of a GaAs MESFET with 1-μm gate length are characterized versus temperature. At room temperature, the noise figure measured at 12 GHz is 3.5 dB. At 90 K, the noise figure decreases to 0.8 dB (T_e = 60 K). The associated gain is 8 dB. The design of a cooled amplifier for the 11.7–12.2-GHz communication band is discussed. At 60 K, the three-stage amplifier exhibits 1.6-dB noise figure (T_e = 130 K) and 31-dB gain.**

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The authors are with the Solid State Laboratory, Hewlett-Packard Company, Palo Alto, CA 94304.

Introduction

At room temperature, thermal noise sources dominate the noise performance of GaAs MESFET's in microwave amplifiers [1], [2]. By cooling the MESFET's to 77 K, a significant noise reduction has been observed in the 1–2-GHz range [3]–[5]. Also, a 2-dB noise-figure reduction has been reported for a 6-GHz MESFET amplifier when cooled to 190 K [6]. The purpose of this short paper is to present MESFET characteristics versus temperature that are relevant to amplifier applications. Based on these device data, the design of a cooled communication amplifier is outlined and the amplifier performance data versus temperature are discussed.

MESFET Performance

The GaAs MESFET discussed in this short paper has been described in [7]. The gate is 1 μm long, 500 μm wide, and the channel is 0.2 μm thick. The active layer was grown by liquid-phase epitaxy directly on the (100) surface of a Cr-doped semi-insulating substrate. The criteria for the selection of the substrate are discussed in [8]. Tin was chosen as the donor impurity which has a negligible ionization energy (similar to sulfur [9]) at 1×10^{17} cm^{-3} doping density. Consequently, the free-carrier concentration in the channel is practically temperature independent.

To characterize the MESFET performance at low temperature, the transistor chip is mounted in a test fixture in which miniature coaxial lines[1] are directly contacting the gate and drain pads on the chip. The source is grounded with 40-pH lead inductance. At 12 GHz, this fixture exhibits less than 0.1-dB insertion loss at the input and output ports. The backside of the MESFET substrate is mounted on a heat sink yielding a thermal resistance of 100 K/W. Under low-noise operating conditions, 100-mW dc power is dissipated in the MESFET, raising the channel temperature approximately 10 K above the ambient temperature. The temperature of the heat sink (ambient temperature) was monitored close to the chip with a copper–constantan thermocouple. The test fixture was suspended above a liquid-nitrogen bath, and the temperature was changed by varying the distance between the fixture and the liquid-nitrogen level.

The noise figure and associated gain of the GaAs MESFET were measured at 12-GHz versus ambient temperature. At each temperature, the gate bias and the RF tuning at the gate and drain[2] were adjusted for minimum noise figure. The solid curves in Fig. 1 show the result. The noise figure decreases from 3.5 dB at 300 K to 0.8 $\pm$ 0.5 dB at 90 K. This performance demonstrates the ultralow-noise capability of cooled GaAs MESFET's at frequencies as high as 12 GHz. The rate of noise-figure decrease is particularly large between 300 and 200 K, which makes thermoelectric cooling an attractive technique for improving noise performance. The gain associated with the minimum noise figure changes from 7.4 dB at 300 K to 8.3 dB at 90 K. With decreasing temperature, the reverse bias on the gate had to be increased to achieve lowest noise performance. At the optimum gate bias, the ratio of the actual drain current, I_{DS}, to the current at zero gate voltage, I_{DSS}, remained approximately independent of temperature for most FET's tested. Using this rule, the optimum gate bias can be determined from simple drain-current measurements on a cooled MESFET providing that the optimum bias at room temperature is known.

The dashed curves in Fig. 1 show the MESFET's noise figure and

[1] The inner conductor has a 100-μm diameter.
[2] The transistor is operated in common-source configuration.